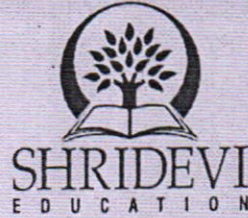


Sri Shridevi Charitable Trust (R.)

# SHRIDEVI INSTITUTE OF ENGINEERING & TECHNOLOGY

(Approved by the AICTE, Affiliated to VTU, Belgaum, Recognized by Govt. of Karnataka.)

TUMAKURU - 572106.



chrg - 39

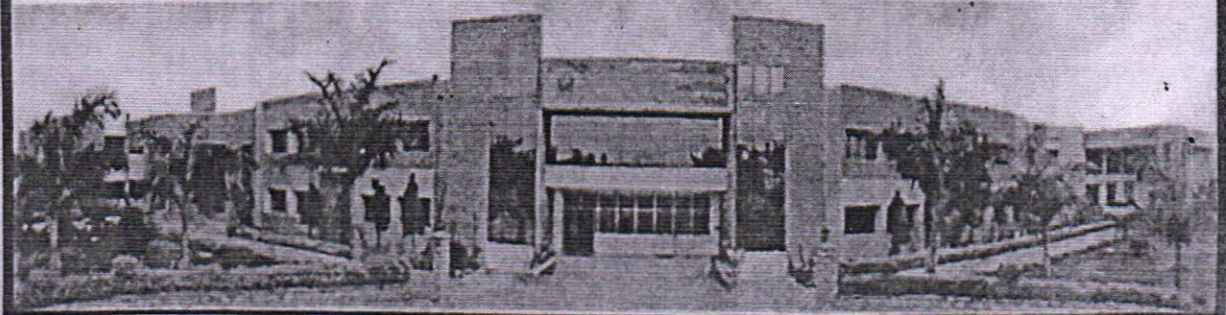
## BLUE BOOK

<b>USN :</b>	1	S	V	1	7	E	C	0	0	3
--------------	---	---	---	---	---	---	---	---	---	---

Name of Student : David S

Course : Microprocessor

Semester : IV Sem Branch : Electronics and Communication



*Manjunath*  
PRINCIPAL  
SIET., TUMAKURU.

### INTERNAL ASSESSMENT MARKS

Date	Test No.	Max. Marks	Marks Obtained	Course Instructor Signature
16/03/19	01	30	28	<i>[Signature]</i> 16/3
16/04/19	02	30	29	<i>[Signature]</i> 16/4
18/5/19	03	30	30	<i>[Signature]</i> 21/5
	Average	30	29	<i>[Signature]</i>

*Assy*      10  

$$\frac{39}{40}$$
*[Signature]* 23/5/19

### CERTIFICATE

This is to certify that Kum/Sri David S  
 with USN 15V17E1003 has satisfactorily completed the course of  
 tests in the subject of Miscoprocessor as prescribed by  
 the Visvesvaraya Technological University for the 2<sup>nd</sup> / I E Sem year / semester  
 B.E. degree course in the year 20 4-2019

*David S*  
 Signature of the Student

*[Signature]* 23/5/19  
 Course Instructor

*[Signature]* 23/5/19  
 Head of the Department

*N. Srinivasan*  
 PRINCIPAL  
 SIET., TUMAKURU.

### TEST NO. 1

Q.No.	a	b	c	d	Total
Q1					
Q2	08	05			13
Q3	08	07			15
Q4		07			07
Q5					
Q6					
Test -1 Marks					28

### TEST NO. 2

Q.No.	a	b	c	d	Total
Q1	7	7			14
Q2					
Q3	6	9			15
Q4					
Q5					
Q6					
Test -2 Marks					29

### TEST NO. 3

Q.No.	a	b	c	d	Total
Q1	8	7			15
Q2					
Q3					
Q4	8	7			15
Q5					
Q6					
Test -3 Marks					30

### REMARKS

---



---



---



---



---



---



---

*Principals Signature*

PRINCIPAL  
SIET, TUMAKURU.

2) a) Addressing modes in 8086 are.

i) Register Addressing mode: Register Addressing mode is the type of Addressing mode in which the Register is used as Destination. The Address of the source is moved to the Register Destination.

ex: `MOV CX, DX`

BE:  $CX = 0009H$

$DX = 0023H$

AE:  $CX = 0023H$

$DX = 0023H$

ii) Based Indexed Addressing mode: The Based Indexed Addressing mode is the type of memory reference Addressing mode in Based Indexed Addressing mode the Address of the source is moved to the Address of Destination.

ex: `MOV [BX], [SI]`

BE:  $[SI] = 0000H = 0239H$

$[BX] = 000EH = 0884H$

AE:

$[BX] = 000EH = 0839H$

$[SI] = 0000H = 0239H$

*Nandha Lakshmi*

PRINCIPAL  
SIET, TUMAKURU.

iii) Immediate Addressing mode: The Immediate Addressing mode is which the Immediate instruction that is Immediate Data is moved to the register. In this the data is moved to the register.

ex: MOV CX, 04H  
MOV DX, 45H

\* BE: DX = 23H or XX

AE: DX = 45H

\* BE: CX = XX

AE: CX = 04H

iv) Direct Addressing mode: The Direct Addressing mode is the type of memory reference Addressing mode in which the data is directly moved to a particular register or destination.

ex: MOV ES, CX  
MOV DS, CX

The data present in the CX register is directly moved to ES and DS Data Segment.

ex: MOV ES, CX  
MOV DS, CX

BE: CX = 0234H

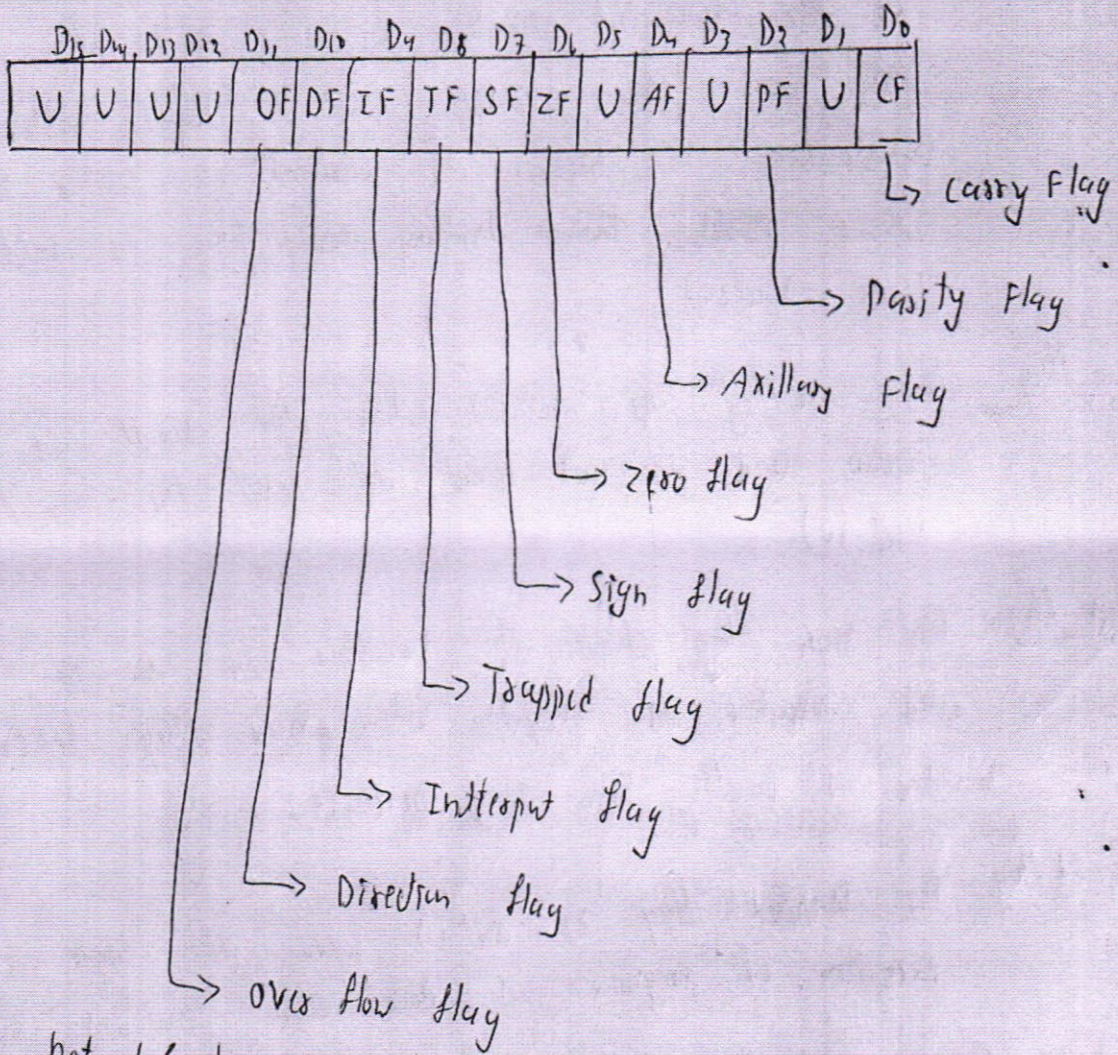
ES = 0000H = XXXX

AE: CX = 0234H

ES = 0000H = 0234H

## 25) The Flag Register of 8086

The Flag Register is which the when the instruction is performed in the operation the flag are checked and it contains some information the block of the Flag register is show below



V is not defined

+ Carry Flag: The carry flag is set when the arithmetic operation is done the result containing carry the carry flag is set (1) other wise set (0)

*Nanda Lakshmi*

PRINCIPAL  
SIET, TUMAKURU.

- \* Parity Flag: The parity flag checks the even and odd number of the result and when the arithmetic instruction is performed the result is even the parity flag is set (1) other wise reset (0)
- \* Axillary Flag: The Axillary carry flag is set (1) when the addition of the two bit number are done and the carry is got from lower nibble and to higher nibble and subtraction the borrow is carryed to higher nibble to lower nibble then Axillary carry flag is set (1) other wise reset (0)
- \* Zero Flag: The zero flag is set (1) when the result is equal to zero and is not equal to zero the zero flag is reset (0)
- \* Sign Flag: The sign flag checks the number is negative or positive and number is negative then sign flag set (1) and number is positive sign flag reset (0)
- \* Trapped Flag: The Trapped flag is set (1) when the single step execution of program is done and reset (0) other wise
- \* Interrupt Flag: The Interrupt flag is set (1) when the instruction INTP is present in the program or else reset (0)
- \* Direction Flag: The Direction flag is set (1) when the result is directed to the other register

*N. Srinivasan*

PRINCIPAL  
SIET, TUMAKURU.

\* overflow flag: when the arithmetic operation is done and then consider 8 bit 2 number to add and store in size of 8 bit only but the result is 32 bit then overflow flag is set (1) or else 0

3.9) i) LEA (Load effective address)

The LEA instruction is used to load the effective address of the source to destination

ex: LEA CX, [SI]

BE: CX = 2309H

[SI] = 00EFH = 8844H

AE: [SI] = 00EFH = 8844H

CX = 8844H

ii) IDIV (Integer Division)

The Integer Division IDIV is used to divide the number of unsigned or negative numbers in DIVS or in DIVD

ex: IDIV Num

IDIV DIVD, DIVS

BE:-

DIVD = -24H

DIVS = 12H

124 = 000011

AE:-

Res = -2H

*Namur Lemayathu*

PRINCIPAL  
SIET, TUMAKURU.



iii) XLAT :- (X Translate Table)

In this XLAT instruction the Translate Table is used and exchange of the data is done between the destination and with the Translate Table

01	0001H
02	0002H
03	0003H
04	0004H
05	0005H
06	0006H
07	0007H

Translate table

Ex: XLAT DX, [SI]

BE:-

[SI] = 0006H = 06H  
DX = 0008H

AE:-

[SI] = 0006H = 0008H  
DX = 06H

iv) DAA (Decimal Adjust Addition):

The DAA instruction is used to adjust the decimal value of the given hexadecimal value the addition is done between the decimal numbers

Ex: DAA (AX, BX)

BE:-

AX = 0364H  
DX = 0584H

AE = 8EF

BX = 0584H

873  
+ 1417  
-----  
2287  
-----  
8EF

3b) To find square of a given number

⇒ code

```
.MODEL SMALL
.DATA
NUM DB 09H
RES DW 00H
.CODE
START: MOV AX, @DATA
        MOV DS, AX
        MOV NUM, 09H
        MOV AX, NUM
        MUL NUM
        MOV RES, AX
        MOV AH, 04CH
        INT 21H
        END START
```

\* Result:

Before Execution

DS:	000EH	NUM	09	00	RES	00	00
-----	-------	-----	----	----	-----	----	----

AE

DS:	000EH	NUM	09	00	RES	81	00
-----	-------	-----	----	----	-----	----	----

*N. Srinivas*

PRINCIPAL  
SIET., TUMAKURU.

.CODE

.MODEL SMALL

.DATA

Num DB 09H

RES DW 00H

.CODE

```
START: MOV AX, @DATA
        MOV DS, AX
        MOV AX, 09H
        MBL Num
        MOV RES, AX
        MOV AH, 04CH
        INT 21H
        EOD START
```

4b) To convert Binary number into gray code

.CODE

.MODEL SMALL

.DATA

Num DB 34H

RES DW 00H

.CODE

```
START: MOV AX, @DATA
        MOV DS, AX
        MOV AL, 34H
        MOV BL, AL
        CLC
        RCR AL, 01H
```

```
XOR bl, al
MOV RES, bl
MOV AH, 04h
INT 21
END START
```

Binary  $\Rightarrow$  cyday code  
3411  $\Rightarrow$  2E11

-07-

*Nandha Kumar*

PRINCIPAL  
SIET., TUMAKURU.

## 2nd Internal Assessment

1a) \* CMPB: (compare string)

The compare string is used in the program to compare string. The DI is compared with SI source and SI subtracted by the DI and SI is updated and CF, PF, SF, ZF affected.

ex:-

$CMPB [SI:DI] \rightarrow [ES:DI]$

BE \*  $CMPB DI$

SI: 0000H

DI: 0000H

PF  $\rightarrow$  0 SF  $\rightarrow$  0 ZF  $\rightarrow$  0

AE

SI: 0001H

DI: 0001H

PF  $\rightarrow$  1 SF  $\rightarrow$  0 ZF  $\rightarrow$  0

\* SCAS (Scan string):

The scan string is used to subtract the SI with the AL or AX and SI is updated and flag register are affected.

$SCAS SI, AL$

ex:-

BE

SI: 0001H

[DX = 45]

AL: 54H

54 - 45

= F

AE

SI: 0001H

[DX = F]

AL: 54H

*N. Srinivasan*

PRINCIPAL  
SIET, TUMAKURU.

\* REPZ: (Repeat if not zero)

The program is repeated if not zero means that the program would not contain zero then the program is repeated

Ex: REPZ AL

\* INTO: (Interrupt overflow)

The overflow flag is set then the interrupt is introduced in the program. Delay is made in the program.

OF flag is set means the interrupt is made in the program.

\* HLT: (Halt)

The Halt is the time delay in the program that is used when exchange operation is done. HLT is used when exchange instruction used between registers. The halt is used.

\* CLD: (Clear Direction flag)

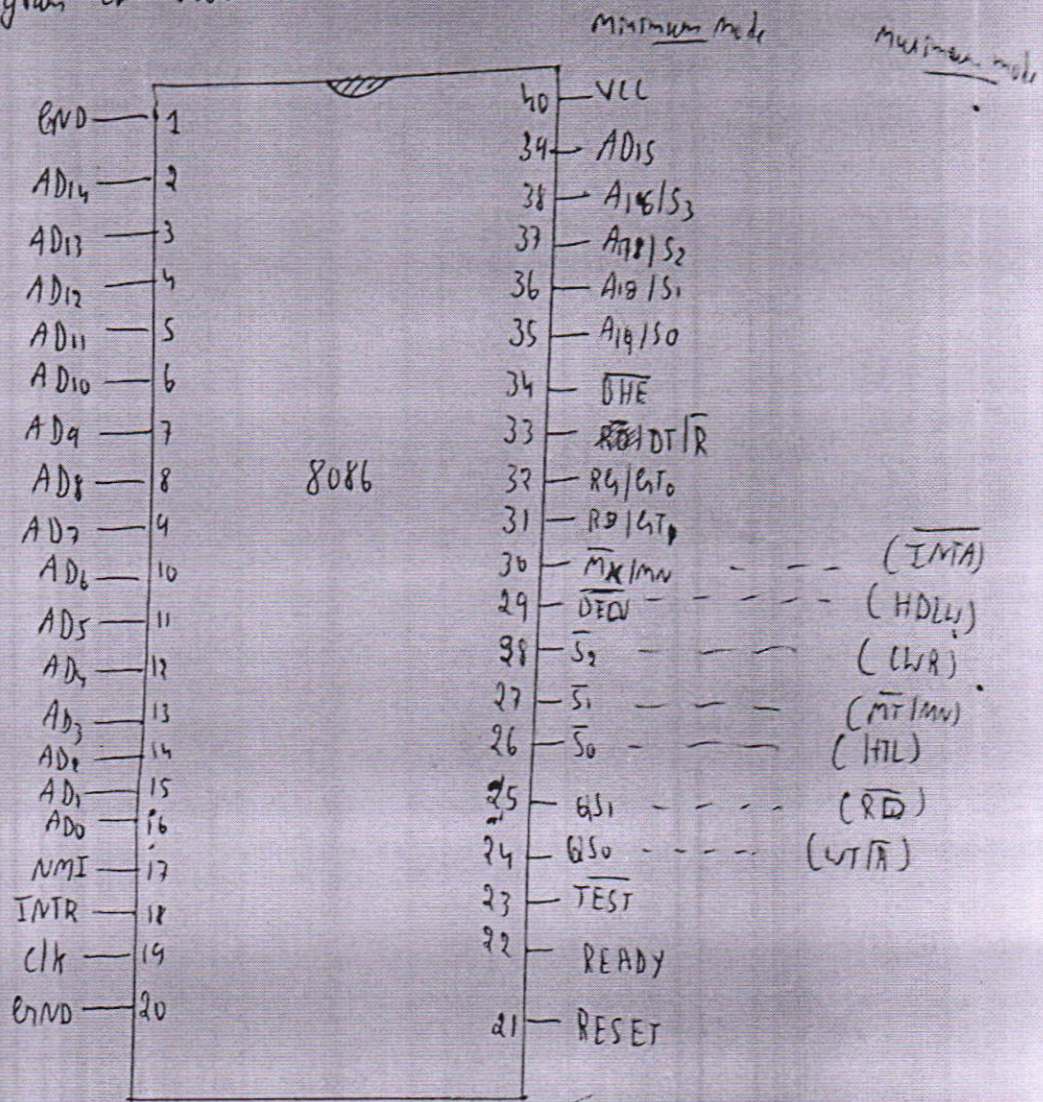
The CLD is used to clear the direction flag and make zero initially.

\* Locks: The Lock is used to hold the program for some time and then it is work properly as it is.

*Nandha Kumar*

PRINCIPAL  
SIET., TUMAKURU.

b) The pin diagram of 8086.



\* The 8086 is worked for the range of the frequency 5.8 and 10 kHz and an VCC supply pin diagram of 8086 is as shown and the memory block and the system control with the pins is explained as follows.

\* GND and VCC: The pin no. 1 and 20 are ground and 40 pin is VCC.  
AD<sub>15</sub> - AD<sub>0</sub> - The pin 39 and 2 to 16 pin are to input and output connection of the 8086 is shown and the S<sub>4</sub> and S<sub>5</sub> are pin selection it work as

*Principals*

PRINCIPAL  
SLET, TUMAKURU.

$S_3$	$S_4$	Indication
0	0	Alternate
0	1	Steady
1	0	code <del>or</del> mode
1	1	None

that is the work of 8086 in that suitable one.

+ NMI (Non maskable Interrupt)

The interrupt is made to an 8086 with out disturbing any other pin mode operation

+  $\overline{CLK}$ :  $\overline{CLK}$  is to give the clock pulse to the 8086.

+  $\overline{BHE}$ : (Bus Data enable)

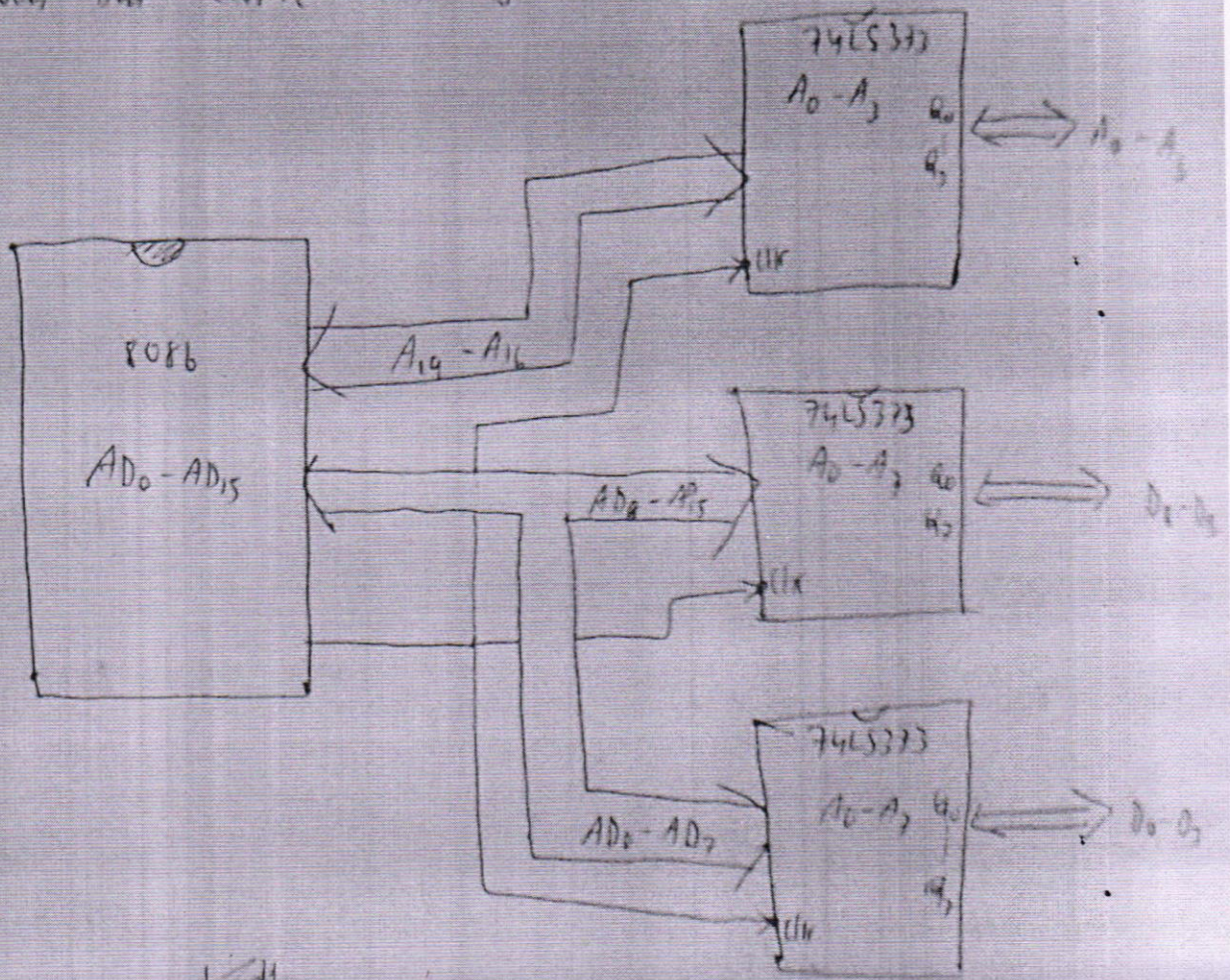
it is active low pin and it transfer the data to the microprocessor and receives the data from the bus.

*N. Srinivas*

PRINCIPAL  
SIET, TUMAKURU.



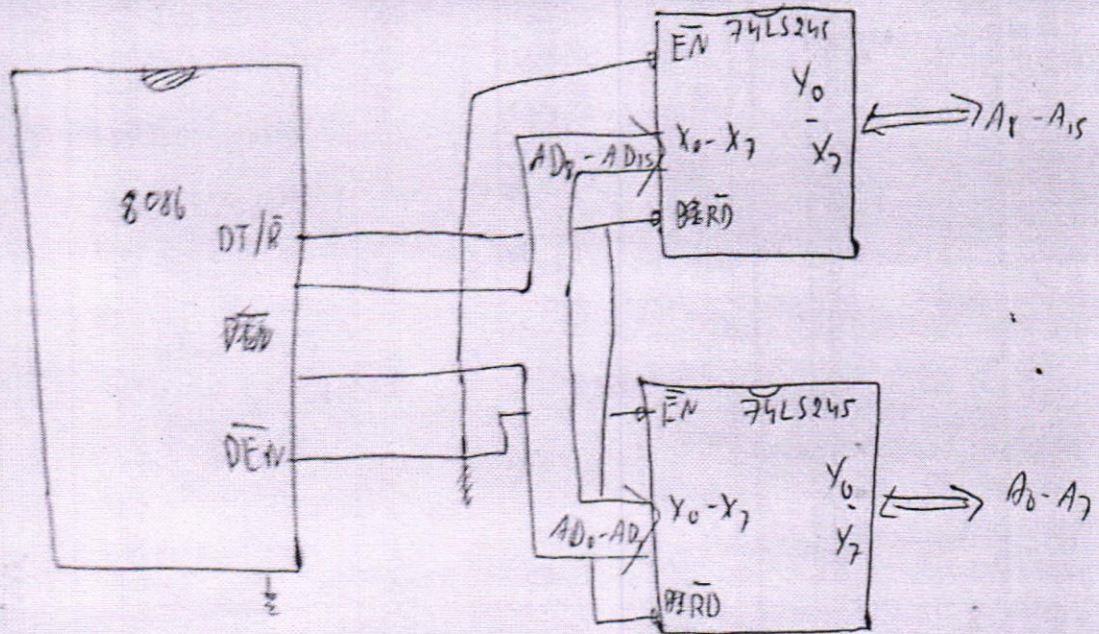
39) Address bus derived from system bus



Latch + Latch output derived from system bus

⇒ The address bus is used to the device through the 74LS373 in a system and  $A_{19}-A_{16}$  address is sent through one IC 74LS373 and  $A_{0}-A_{15}$  is divided  $A_{0}-A_{7}$   $A_{8}-A_{15}$  is sent through one two different IC 74LS373.

*Manjunath*  
 PRINCIPAL  
 SIET, TUMAKURU.



\* Data bus derived from system bus

The Data bus is needed via 74LS245 IC taken two IC's and send  $A_0-A_7$  is one, and  $A_8$  to  $A_{15}$  is another IC.  $\bar{DEN}$  is correct and  $DT/\bar{R}$  is correct as shown in the block diagram of Data bus.

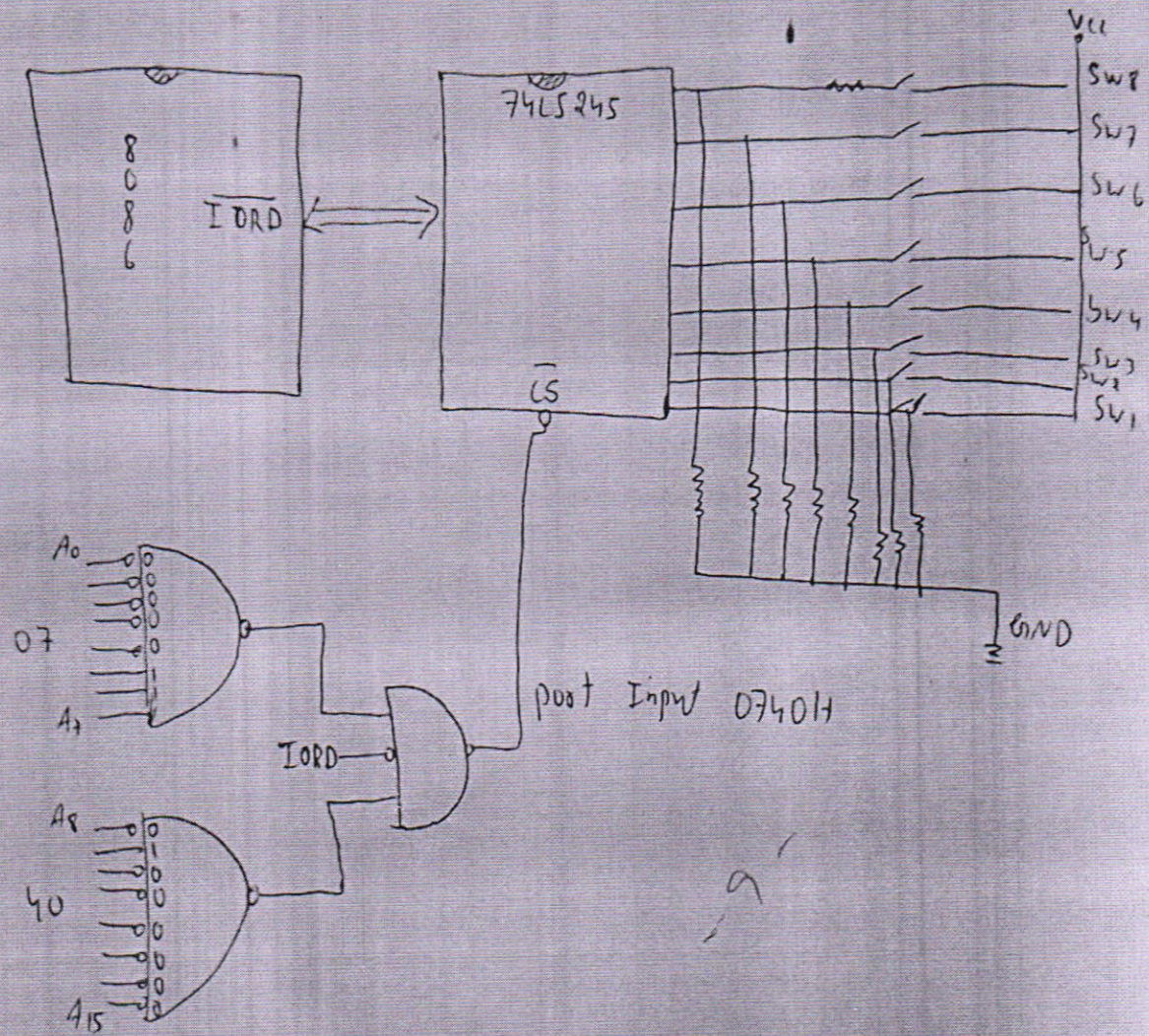
6

5b)

⇒ Program:

```

MOV BL, 00H      (Move 00H to BL)
MOV DX, 0740H   (Move 0740H to DX)
IN AL, DX
MOV BL, AL      (Move AL to BL)
HLT              (Halt)
    
```



1 a) Interrupt vector table :

Types	ISR	IP	CS;	Address	
Type 0	}	ISR	IP	000011	} Received <del>by</del> divided by zero
			CS;	0000211	
Type 1	}	ISR	IP	0000411	} Received for single step instructions
			CS;	0000611	
Type 2	}	ISR	IP	0000811	} Received for NMI
			CS;	0000A11	
Type 3	}	ISR	IP	0000C11	} Received for INT Single bit instructions
			CS;	0000E11	
Type 4	}	ISR	IP	0001011	} Received for INTO instructions
			CS;	0001211	
		:	:	:	
		:	:	:	
Type N	}	ISR	IP	004A11	} Received for INT 2 byte instructions
			CS;	004A211	
		:	:	:	
		:	:	:	
Type FF	}	ISR	IP	003FE11	
			CS;	003FF11	

FF = 255 interrupts

\* Interrupt vector table \*

⇒ The interrupt vector table is as shown. The interrupt is recognized that which type of interrupt that is Type 0 to Type N it indicates whether the interrupt is performed or not that is Type 0 when Type 0 interrupt is recognized it is divided by zero from so the program will be interrupted and terminated.

When Type 1 is recognized in the INT single bit instruction that make some delay in the program. Type 2 is recognized it is for NMI (non maskable interrupt) that is having separate pin in the 8086 IC and it is active high pin. When Type 3 is recognized that the system having Int signal for a single bit instruction. Type 4 when Type 4 interrupt is recognized it is for INTR instruction that is active low pin in the 8086 IC that is 0 and active and to interrupt the program.

\*  $\Rightarrow$  The interrupt vector table consisting of types of interrupt and address and comments that is for which type which interrupt is position and the address starts from 00000 to 003FFH and interrupt vector table having Type FF interrupts, that is 255 interrupts.

b) 100ms, 10MHz frequency.

$\Rightarrow$  The required Delay  $T_d = 100ms$

The working frequency of 8086 = 10MHz

$$\text{Time } T = \frac{1}{f} = \frac{1}{10M} = 100nSec = 0.1mSec$$

\* Delay program:-

MOV CX, count	4	} Delay
DEC CX	2	
NOP	3	
JNZ table	16	
	<u>21 = n</u>	

\*  $2 + 3 + 16 = 21 = n$   
 $n = 21$  for the Delay program.

The count of  $N = \frac{T_d}{n \times T} = \frac{100ms}{21 \times 0.1m} = 47619 \text{ (BA03)}$

⇒ The count N in decimal 47619 is converted into hexadecimal BA03

\* Calculation:

$$\text{Delay} = 4 \times 0.1\mu \times \text{BA03} + 2 \times 0.1\mu \times \text{BA03} + 3 \times 0.1\mu \times \text{BA03} + 16 \times 0.1\mu \times \text{BA03}$$

$$\text{Delay} = 0.4\mu + 9.5238\mu + 0.0142857 + 0.0761904$$

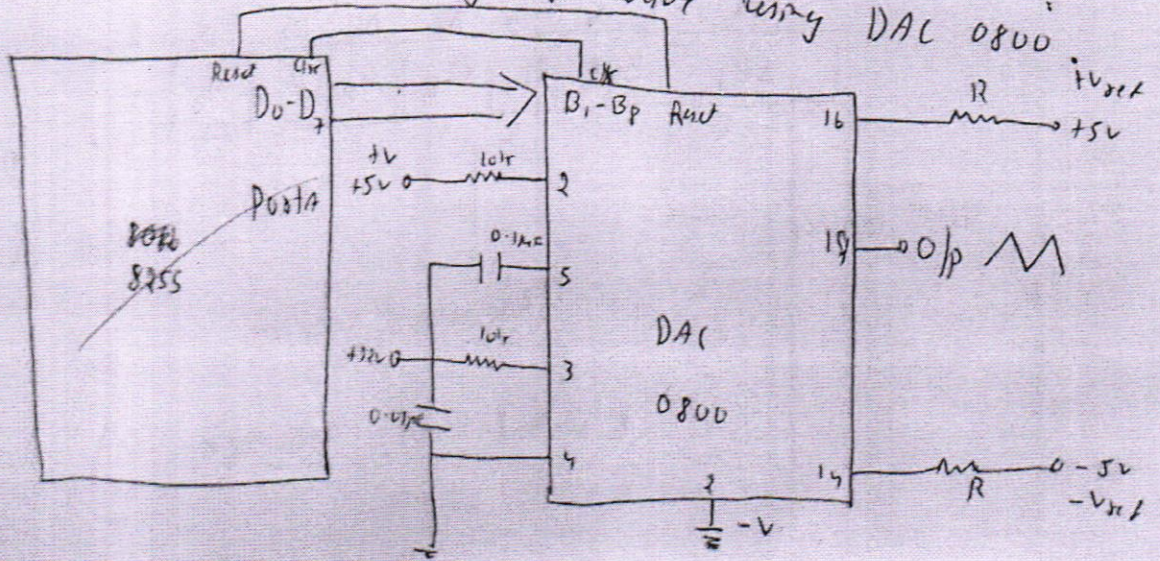
$$\text{Delay} = 100 \times 10^{-3}$$

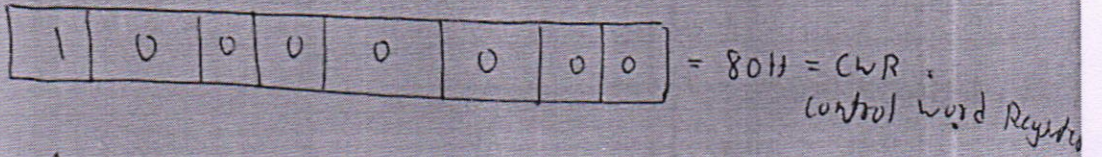
$$\text{Delay} = \underline{\underline{100\text{mSec}}}$$

\* program:

⇒ Assume CS: code  
Code Segment  
MOV CX, BA03 → 4  
Wait: DEC CX → 2  
NOP → 3  
JNZ Wait → 16  
RET → 4  
code ENDS → 8  
END proc

4a) program to generate triangular wave using DAC 0800

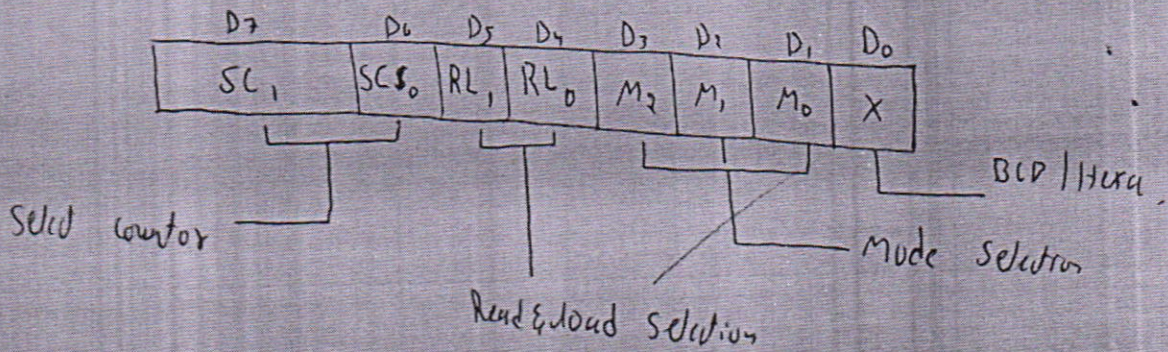




```

program:
  Assume CS: code
  code segment
  start: mov AL, 80H
        out CWR, AL
        mov AL, 00H
  backr: out portA, AL
        inc AL
        cmp AL, FFH
        jB backr
  backr1: out portA, AL
         dec AL
         cmp AL, 00H
         JA backr1
         jmp backr
  code ends
  end start
  
```

45) Control word register of 8254 timer.



+ Control word register +

*Nandan Kumar*

PRINCIPAL  
SIET., TUMAKURU.

\*  $D_0$  - Least selection

Bcd	1
Hexa decimal	0

\*  $SC_1$  &  $SC_0$  (Select counter)

$SC_1$	$SC_0$	operation
0	0	Counter 0
0	1	Counter 1
1	0	Counter 2
1	1	Illegal

\* RL (Read / Load selection)

$RL_1$	$RL_0$	operation
0	0	No operation
0	1	Read and Load LPSB only
1	0	Read and Load MSB only
1	1	Read and load LSB first then MSB

where LSB  $\rightarrow$  Least Significant byte  
MSB  $\rightarrow$  Most significant byte

\* Mode Selection:

$M_2$	$M_1$	$M_0$	operation
0	0	0	mode 0
0	0	1	mode 1
X	1	0	mode 2
X	1	1	mode 3
1	0	0	mode 4
1	0	1	mode 5

*Principals Signature*

PRINCIPAL  
SIET, TUMAKURU.



\* The control word register of 8254 timer is as shown and the working of the Bits  $D_0$  to  $D_7$  is shown in the table of modes and select counter and Read and Load selection tables that is the  $D_0$  bit is 1 for BCD count and 0 for Hexadecimal count and Modes  $M_2$ ,  $M_1$ , &  $M_0$  bit  $D_{13}$ ,  $D_2$  and  $D_{21}$  is selected as in the table of mode selection, and bit  $D_{15}$  and  $D_{14}$  is the Read and Load the LSB and MSB of the counter that is shown in table Read and Load select. and bit number  $D_7$  and  $D_6$  for select counter that is done as in the table following

$SC_1$	$SC_0$	operation
0	0	counter 0
0	1	counter 1
1	0	counter 2
1	1	Illegal

*N. Srinivasan*  
 PRINCIPAL  
 SIET., TUMAKURU.