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ESTD:2002
20 YEARS Academic Excellence
(Approved by AICTE, New Delhi, Recognised by Govt. of Karnataka and Affiliated to Visvesvaraya Technological University, Belagavi)

Curriculum for ASIC based VLSI designCourse

Introduction to

- VLSI Design Flow
- ASIC Vs FPGA
- RTL Design Methodologies
- Introduction to ASIC Verification Methodologies
- VLSI Design Flow Steps - Demo

Advanced Digital Design

- Introduction to Digital Electronics
- Arithmetic Circuits
- Data processing Circuits
- Universal Logic Elements
- Combinational Circuits - Design and Analysis
- Latches and Flip flops
- Shift Registers and Counters
- Sequential Circuits - Design and Analysis
- Memories and PLD
- Finite State Machine
- Microcontroller Design

Static Timing Analysis

- Introduction to STA
- Comparison with DTA
- Timing Path and Constraints
- Different types of clocks

- Clock domain and Variations
- Clock Distribution Networks
- How to fix timing failure

CMOS Fundamentals

- Non Ideal characteristics
- BJT vs FET
- CMOS Characteristics
- CMOS circuit design
- Transistor sizing
- Layout and Stick Diagrams
- CMOS Processing Steps
- Fabrication
- CMOS Technology - Current Trends

Assessment: Students should obtain

Min 80% of attendance

Min 80% Participation in practice session

Quiz

Coordinator

HOD

HOD
Dept of E&C
SIET, Tumkur-6

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